REMARKS

The Applicant provides the following comments to supplement the arguments made in the previous Response.

Claims 1-12 and 15 have been rejected under 35 U.S.C. 102(e) as being anticipated by Ohtani (US 20030157758). Claims 13-14, which depend from Claim 1, are allowable over Ohtani for at least the same reasons as Claim 1.

Claim 1 recites "forming one or more diffusion bit line regions in a semiconductor substrate; then thermally oxidizing the upper surface of the semiconductor substrate, thereby forming a bottom oxide layer over the upper surface of the semiconductor substrate and simultaneously forming bit line oxide regions over each of the one or more diffusion bit line regions; and then forming an intermediate dielectric layer over the bottom oxide layer and the bit line oxide regions." (Emphasis added.)

In the Response to Arguments, the Examiner insists that the sequence required by Applicant's Claim 1 is taught by Ohtani. More specifically, the Examiner argues that Ohtani teaches that "layer 3 is formed before layer 5, which is formed before layer 9 as described in detail in paragraphs 0010 and 0011". This is simply not true.

A. 'Layer 3' is not formed before 'Layer 9'

Paragraph 0010 of Ohtani states:

> In order to gain the structure shown in FIG. 65, ONO film 9 is formed over the entirety of semiconductor substrate 1 and a plurality of buried diffusion bit lines 3 are formed by selectively implanting n-type impurities into semiconductor substrate 1 …" (Ohtani, paragraph 0010.)

This section of Ohtani does not indicate that buried diffusion bit lines 3 are formed before ONO film 9. In

fact, Ohtani first discusses the formation of ONO film 9, and then discusses the formation of diffusion bit lines 3. Paragraph 0004 of Ohtani explicitly indicates that the semiconductor device of FIG. 65 is described in U.S. Patent No. 6,174,758 to Nachumovsky. As described in Applicant's previous response, U.S. Patent No. 6,174,758 explicitly teaches the formation of an ONO structure, followed by the formation of diffusion bit lines, followed by the formation of bit line oxide. (U.S. Patent No. 6,174,758, Figs. 4-7.) Thus, Ohtani teaches that the buried diffusion bit lines 3 are formed after ONO film 9.

Because Ohtani teaches that the buried diffusion bit lines 3 are formed after ONO film 9, Ohtani fails to teach "forming one or more diffusion bit line regions … then … forming a bottom oxide layer … and then forming an intermediate dielectric layer over the bottom oxide layer" as recited by Applicant's Claim 1. For this reason, Ohtani does not anticipate Applicant's Claim 1.

B. 'Layer 5' is not formed before 'Layer 9'

In addition, paragraph 0010 of Ohtani states:

> ONO film 9 is formed … and a plurality of buried diffusion bit lines 3 are formed … and, ***after that***, thermal oxidation is carried out so as to form bit line oxidized regions 5 …". (Emphasis added.) (Ohtani, paragraph 0010.)

Thus, paragraph 0010 of Ohtani explicitly teaches that bit line oxidized regions 5 are formed after ONO film 9. For this reason, Ohtani does not teach that bit line oxidized regions 5 are formed before ONO film 9 as suggested by the Examiner.

Because Ohtani teaches that the bit line oxidized regions 5 are formed after ONO film 9, Ohtani fails to teach "forming bit line oxide regions … and then forming an intermediate dielectric layer over the bottom oxide layer and the bit line oxide regions" as recited by Applicant's Claim 1. For this additional reason, Ohtani does not anticipate Applicant's Claim 1.

The 'Response to Arguments' also states: "Applicant argues that layer 9 and layer 20 should constitute a 103 rejection, this is not persuasive because layers 9 and 20 are taught in the prior art figure". (Emphasis added.)

Contrary to the Examiner's assertion, layers 9 and 20 are not taught in the prior art figure (i.e., FIG. 65 of Ohtani). More specifically, prior art FIG. 65 of Ohtani does not include a layer 20. Layer 20 is only found in non-prior art figures of Ohtani (e.g., Fig. 63). The Applicant's original Response simply indicated that it is improper to randomly combine elements of the prior art and elements of the invention of Ohtani without some showing of motivation to combine.

The 'Response to Arguments' also does not address all of the Applicant's arguments. For example, the Examiner has not addressed the argument that Figure 63 of Ohtani is directed toward the deposition of a polysilicon film 33, and does not seem to teach or suggest forming "an intermediate dielectric layer" as recited by Claim 1. The Examiner has also not addressed the argument that the process sequence including Figure 63 of Ohtani forms the bit line oxide films "by means of a CVD method or the like", and therefore explicitly teaches away from "thermally oxidizing the upper surface of the semiconductor substrate" as recited by Claim 1.

For the above-described reasons, Claim 1 is not anticipated by Ohtani. Claims 2-12 and 15, which depend from Claim 1, are not anticipated by Ohtani for at least the same reasons as Claim 1.

In addition, the Examiner has not addressed the argument that Ohtani teaches that the CMOS well regions are formed before ONO structure 9, and therefore fails to teach "implanting CMOS well regions through the intermediate dielectric layer and the bottom oxide layer" as recited by Claim 7.

Claims 13-14, which depend from Claim 1, are allowable over Ohtani for at least the same reasons as Claim 1.

CONCLUSION

Claims 1-15 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested. If there are any questions, please telephone the undersigned at (925) 895-3545 to expedite prosecution of this case.

Respectfully submitted,

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